Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANNY R. CLINE

Appeal No. 1997-2247
Application No. 08/259,798

ON BRIEF

Before HAIRSTON, JERRY SMITH, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the rejection of claims 1-12. We affirm-in-part.

BACKGROUND

The invention at issue in this appeal relates to stress testing an integrated circuit (IC) memory. Stress testing is commonly used to learn when an IC memory is expected to fail prematurely during normal use. Because only a few of tens of

thousands of word lines of the memory typically have been asserted at a time and only half of the bit lines, i.e., either the true or complement bit lines, of the memory typically have been driven to a desired voltage level at a time, such testing has proven time consuming.

The invention speeds stress testing of an IC memory. Specifically, a control signal is applied to the necessary predecoders and row factor generators to enable all word lines of the memory simultaneously. The signal is also applied to disable the sense amplifiers of the memory. In addition, all bit lines, i.e., both the true and complement bit lines, of the memory are initialized as the control signal clamps a bit line voltage reference to a Vss voltage. These operations effectively write zeros across the whole memory at once and provide a proper bias on the cells of the memory for testing.

Claim 1, which is representative for our purposes, follows:[1]

> 1. A circuit comprising:
> an array of storage cells arranged in rows and columns;
> a plurality of wordlines, each wordline connected with gates of transfer transistors of a different row of the storage cells;
> a node for receiving a supply voltage;
> a decoder, responsive to a control signal, for simultaneously applying the supply voltage to all of the wordlines of the array.

The references relied on in rejecting the claims follow:

Hardee et al. (Hardee)	4,680,762	July 14, 1987
Kuo et al. (Kuo)	5,034,923	July 23, 1991.

Claims 1-4 stand rejected under 35 U.S.C. § 103 as obvious over Hardee. Claims 5-9 and 12 stand rejected under 35 U.S.C. § 103 as obvious over Hardee in view of Kuo. Claims 10 and 11 stand rejected under 35 U.S.C. § 103 as obvious over Kuo. Rather than repeat the arguments of the appellant or examiner in toto, we refer the reader to the brief and answer for the respective details thereof.

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[1]The copy of claim 1 that appears in Appendix A of the brief is inaccurate.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellant and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 1-4 as obvious over Hardee and claims 5-9 and 12 as obvious over Hardee in view of Kuo. We are also persuaded, however, he did not err in rejecting claims 10 and 11 as obvious over Kuo. Accordingly, we affirm-in-part.

We begin by noting the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

> In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).... "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

> If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

With these principles in mind, we consider the rejection of claims 1-9 and 12.

Claims 1-9 and 12

Recognizing that Hardee does not show simultaneous application of a voltage to all the word lines of a storage array, the examiner opines, "[i]t would have been obvious ... to realize that the voltage can also be simultaneously being [sic] applied to each of Hardee's word lines." (Examiner's Answer at 3.) The appellant argues, "Hardee et al. simply contains no teachings or suggestion of simultaneous voltage application to wordlines. Hardee et al. expressly teaches sequential voltage application to its wordlines." (Appeal Br. at 3.)

Claims 1-9 and 12 each specify in pertinent part the following limitations: "an array of storage cells arranged in rows and columns; ... a decoder, responsive to a control

signal for simultaneously applying the supply voltage to all of the wordlines of the array." Accordingly, the limitations require simultaneously applying a supply voltage to all the word lines of a storage array.

The examiner fails to show a suggestion of the limitations in the prior art. He admits, "Hardee does not show the voltage is simultaneously applied to all of the word lines." (Examiner's Answer at 3.) For its part, the reference teaches sequentially applying a voltage to each word line of a storage array. Specifically, "at least one period of the sawtooth voltage waveform applied to pad **20** is applied to each word line in memory array **40**. This may be effectuated by sequentially addressing the word lines of array **20** through the operation of row address buffers **46** and row decoders **48**." Col. 5, ll. 49-54. Faced with this omission, the examiner opines, "[i]t would have been obvious ... to realize that the voltage can also be simultaneously being [sic] applied to each of Hardee's word lines. Such realization is well-known in the

art due to time efficiency for applying voltage into a memory array." (Examiner's Answer at 3.)

"Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995)(citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992)(citing In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991)).

We also note the following principles from In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)(exemplary citations omitted).

> The range of sources available, however, does not diminish the requirement for actual evidence. That is, the showing must be clear and particular. See,

> e.g., C.R. Bard, 157 F.3d at 1352, 48 USPQ2d at 1232. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence."

Although couched in terms of combining prior art references, the same requirement applies in the context of modifying such a reference. Here, the examiner's broad, conclusory opinion of obviousness does not meet the requirement for actual evidence. His allusion to "time efficiency" smacks of impermissible reliance on the appellant's teaching of "time saving procedures ...." (Spec. at 3.) The examiner fails to allege, let alone show, that Kuo remedies the defects of Hardee.

Because Hardee teaches sequentially applying a voltage to each word line and the examiner has not provided any evidence that would have suggested simultaneous application, we are not persuaded that teachings from the prior art would appear to have suggested the claimed limitations of "an array of storage cells arranged in rows and columns; ... a decoder, responsive to a control signal for simultaneously applying the supply voltage to all of the wordlines of the array." The examiner

has failed to establish a prima facie case of obviousness. Therefore, we reverse the rejections of claims 1-4 as obvious over Hardee and claims 5-9 and 12 as obvious over Hardee in view of Kuo. Next, we address the rejection of claims 10 and 11.

Claims 10 and 11

We begin by finding that the references represent the level of ordinary skill in the art. See In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (finding that the Board of Patent Appeals and Interference did not err in concluding that the level of ordinary skill was best determined by the references of record); In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("[T]he PTO usually must evaluate ... the level of ordinary skill solely on the cold words of the literature."). Of course, "'[e]very patent application and reference relies to some extent upon knowledge of persons skilled in the art to complement that [which is] disclosed ....'" In re Bode, 550 F.2d 656, 660, 193 USPQ 12, 16 (CCPA 1977) (quoting In re Wiggins, 488 F.2d 538, 543, 179 USPQ 421, 424 (CCPA 1973)). Those persons "must

be presumed to know something" about the art "apart from what the references disclose." In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA 1962). With this principle in mind, we consider the examiner's rejection and the appellant's arguments.

> The examiner makes the following rejection.
>
> Kuo, suggests that the bit line precharging apparatus (13), in responsive to control lines (14) from a control logic (15), precharges bit lines BL and BL* to high or low logic states .... Such bit lines BL and BL* are a complementary pair of bit lines. In addition, Kuo's precharging apparatus not only can supply a high voltage to the complementary pair of bit lines, but also can supply a low voltage to the complementary pair of bit lines. Such a precharging apparatus would disable a (ie. Low) voltage and supply another (ie. High) voltage to the bit line pair. This is because the precharging apparatus (13), in responsive [sic] to the control lines, has capability [sic] for alternating the voltage (to high or low states ...) on the complementary pair of bit lines.

(Examiner's Answer at 8-9.) The appellant makes two arguments. First, he argues, "Kuo et al. has no teachings or suggestions of precharging the complementary pairs of bitlines. Kuo et al. precharges only one bitline." (Appeal Br. at 4.)

"In the patentability context, claims are to be given their broadest reasonable interpretations. Moreover, limitations are not to be read into the claims from the specification." In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993)(citing In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)). Here, claim 10 specifies in pertinent part the following limitations:

> a plurality of complementary pairs of bitlines ...;
> a precharge circuit for simultaneously precharging both leads of each of the plurality of pairs of bitlines to a common precharge voltage ....

Similarly, claim 11 specifies in pertinent part the following limitations:

> a plurality of complementary pairs of bitlines ...; and
> a circuit arranged for simultaneously precharging both leads of each of the plurality of pairs of bitlines to a common precharge voltage ....

Giving the claims their broadest reasonable interpretation, the limitations recite a precharge circuit for simultaneously precharging both bit lines of a complementary pair of bitlines to a precharge voltage.

Kuo would have suggested the limitations. "[A] disclosure that anticipates under Section 102 also renders the claim invalid under Section 103, for 'anticipation is the epitome of obviousness.'" Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983) (quoting In re Fracalossi, 681 F.2d 792, 215 USPQ 569 (CCPA 1982)). In other words, obviousness follows from an anticipatory reference. RCA Corp. v. Applied Digital Data Sys, Inc., 730 F.2d 1440, 1446, 221 USPQ 385, 390 (Fed. Cir. 1984).

Here, Kuo teaches a precharge circuit for simultaneously precharging both bit lines of a complementary pair of bitlines to a precharge voltage. Specifically, "control logic **15** directs bit line precharge apparatus **13** ... to precharge bit lines **BL** and **BL*** ... to a high logic state." Col. 6, ll. 58-61. See also col. 7, ll. 19-21 ("Control logic **15** directs precharge apparatus **13** to precharge bit lines **BL** and **BL*** to a high logic state ...."); id. at ll. 44-45 ("The access proceeds as a normal write access, with both data lines and

bit lines precharged high ...."). Precharging to the high logic state necessarily requires precharging to a high logic precharging voltage. We are persuaded that these teachings would have suggested ipso facto the limitations of "a plurality of complementary pairs of bitlines ...; a precharge circuit for simultaneously precharging both leads of each of the plurality of pairs of bitlines to a common precharge voltage ..." as well as "a plurality of complementary pairs of bitlines ...; and a circuit arranged for simultaneously precharging both leads of each of the plurality of pairs of bitlines to a common precharge voltage ...."

Second, the appellant argues, "Kuo et al. has no teachings or suggestions of supplying an alternative voltage to both bitlines of each complementary pair. Kuo et al. expressly teaches not writing any value to its complementary bit line." (Appeal Br. at 4.)

Claim 10 specifies in pertinent part the following limitations:

> a precharge disabling circuit, responsive to a control signal, for disabling the precharge circuit from applying the common precharge voltage and for concurrently supplying an alternative common voltage to both leads of each of the plurality of pairs of bitlines ....

Claim 11 similarly specifies in pertinent part the following limitations:

> a circuit arranged for simultaneously precharging both leads of each of the plurality of pairs of bitlines to a common precharge voltage and, in response to a control signal, supplying concurrently an alternative common voltage to both leads of each of the plurality of pairs of bitlines.

Giving the claims their broadest reasonable interpretation, the limitations recite disabling the precharging voltage and supplying an alternative voltage to both of the bit lines.

Kuo would have suggested the limitations. As mentioned regarding the first argument, the reference teaches that the bit line precharge apparatus 13 precharges bit lines BL and BL* to a high logic precharging voltage. In addition, Kuo teaches disabling the high logic precharging voltage and supplying an alternative common voltage to both bit lines BL and BL*. Specifically, "precharge apparatus **13** ... is capable

of precharging bit lines **BL** and **BL*** to high or low logic states." Col. 5, ll. 24-26. Precharging to the low logic state necessarily requires disabling the high logic precharging voltage and supplying an alternative low logic voltage.

We are persuaded that these teachings would have suggested the limitations of "a precharge disabling circuit, responsive to a control signal, for disabling the precharge circuit from applying the common precharge voltage and for concurrently supplying an alternative common voltage to both leads of each of the plurality of pairs of bitlines" and "a circuit arranged for simultaneously precharging both leads of each of the plurality of pairs of bitlines to a common precharge voltage and, in response to a control signal, supplying concurrently an alternative common voltage to both leads of each of the plurality of pairs of bitlines." Therefore, we affirm the rejection of claims 10 and 11 as obvious over Kuo. Our affirmance is based only on the arguments made in the briefs. Arguments not made therein are not before us, are not at issue, and are considered waived.

CONCLUSION

In summary, the rejection of claims 1-4 under 35 U.S.C. § 103 as obvious over Hardee and the rejection of claims 5-9 and 12 under 35 U.S.C. § 103 as obvious over Hardee in view of Kuo are reversed. The rejection of claims 10 and 11 under 35 U.S.C.
§ 103 as obvious over Kuo, however, is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

LLB/kis

Richard B. Havill
TEXAS INSTRUMENTS INCORPORATED
P. O. Box 655474 M/S 219
Dallas, TX 75265